AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A frequency synthesizer, comprising:

a digitally controlled oscillator, including multiple groups of switched capacitors;

multiple control circuits each coupled to a respective one of said groups of capacitors, where the multiple control circuits sequentially control the respective groups of capacitors responsive to a phase error signal during sequential modes; and

a phase detection circuit for generating the phase error signal, said phase detection circuit including circuitry for setting the phase error signal to a predetermined value responsive to a mode switch signal.

2. (Original) The frequency synthesizer of claim 1 wherein said phase detection circuit also sets the phase error signal to the predetermined value responsive to a startup control signal.

3. (Original) The frequency synthesizer of claim 1 wherein said phase detection circuit includes multiple phase calculators.

4. (Original) The frequency synthesizer of claim 3 wherein each of said multiple phase calculators generate a respective phase output and wherein said phase detection circuit further includes circuitry for generating the phase error signal from the phase outputs using a predetermined formula.

5. (Currently amended) The frequency synthesizer of claim 4 wherein one of said phase calculators, responsive to said mode switch signal, generates its phase output from the phase outputs of the other phase calculators using a second predetermined formula.

6. (Original) The frequency synthesizer of claim 5 wherein generating the phase output using said second predetermined formula minimizes the phase error.

7. (Original) The frequency synthesizer of claim 5 wherein said one phase calculator comprises:

circuitry for calculating a first phase output by accumulating a frequency control word;

circuitry for calculating a second phase output using said second predetermined formula; and

circuitry for switching between said first and second phase outputs.

8. (Original) The frequency synthesizer of claim 1 wherein one or more of said control circuits include circuitry for maintaining an output to its respective group of capacitors at the end of a mode.

9. (Currently amended) A method of generating a desired frequency, comprising the steps of:

controlling a multiple groups of switched capacitors in a digitally controlled oscillator responsive to a phase error signal, using respective multiple control circuits each coupled to a respective one of said groups of capacitors, said control circuits operating sequentially during sequential modes;

generating the phase error signal during said modes and setting the phase error signal to a predetermined value responsive to a mode switch signal.

10. (Original) The method of claim 9 wherein said generating step also sets the phase error signal to the predetermined value responsive to a startup control signal.

11. (Original) The method of claim 9 wherein said generating step includes the step of calculating multiple phase measurements.

12. (Original) The method of claim 11 wherein said generating step includes the step of calculating the phase error signal from the phase measurements using a predetermined formula.

13. (Currently amended) The method of claim 12 and further comprising the step of setting one of said phase measurements ~~is set~~ to a value based on the other phase measurements using a second predetermined formula responsive to said mode switch signal.

14. (Original) The method of claim 13 wherein said step of setting one of the phase measurements to a value based on the other phase measurements causes a minimal phase error.

15. (Currently amended) The method of claim 13 wherein said step of setting said one of said phase measurement comprises the steps of:

calculating a first phase output by accumulating a frequency control word;

calculating a second phase output using said second predetermined formula; and

switching between said first and second phase outputs.

16. (Currently amended) The method of claim 9 ~~and~~ further comprising the step of maintaining an output to a respective group of capacitors at the end of a mode.

17-18. (Canceled).